REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

Response to Rejections Under 35 U.S.C. § 112

The rejection of claim 12 under 35 U.S.C. 112, second paragraph, has been addressed by amending claim 12 to depend from claim 1 rather than canceled claim 5.

Additional Claim Amendments

The preamble of claim 1 has been amended to recite reconfiguring internal processing elements into functional units, as recited in the body of the claim, in order to provide proper antecedent basis for the functional units recited in claims 7 and 15, and by amending claims 8-10 to recite "operations" in order to conform to the terminology used in the specification (see, *e.g.*, page 7, line 22) and improve clarity.

Because the amendments are formal in nature and/or are clearly supported by the original specification, it is respectfully submitted that they do not involve "new matter."

Response to Rejections Under 35 U.S.C. § 102

The rejection of claims 1, 3, 4, 7-16 and 18-20 under 35 U.S.C. § 102(b) as being anticipated by Mirsky, 6,226,735 is respectfully traversed on the grounds that the Mirsky patent does not disclose or suggest the inventive feature of using a reconfigurable apparatus with a plurality of processing elements (PE) to provide various

functional units which can be an adder, an ALU, a multiplier (amended claim 1) and even a divider, a floating adder, a floating multiplier (amended claim 15). Instead, the Mirsky patent discloses a PE made up of various functional units, which can be reconfigured to perform various functions. It is respectfully submitted that a PE made up of various functional units that allow the PE to perform different functions is not the same as the claimed combination of PEs to form different functional units, the former suffering from the problem of wasted hardware because not all of the functional units *within* the PEs are used.

According to the Examiner, "*Fig. 3 shows using a pluralityh of MCPEs, note Fig. 2 which shows the details of a MCPE, to create a network processing structure,. . ..*" It appears that the Examiner has misinterpreted Fig. 3 of the Mirsky patent. Instead, of showing multiple PEs, Fig. 3 of Mirsky shows the internal structure of a single "MCPE," as explained in col. 5, lines 21-33:

> *The structure of each MCPE allows for a great deal of flexibility when using the MCPEs to create networked processing structures. FIG. 3 is a data flow diagram of the MCPE of one embodiment. The major components of the MCPE include static random access memory (SRaM) main memory 302, ALU with multiplier and accumulate unit 304. . ..*

Thus, Fig. 3 of Mirsky does not show multiple PEs combined to form an adder, multiplier, or ALU, but rather shows a single PE made up of an ALU, multiplier, and other elements. The result is a very flexible PE, but one which will inevitably include wasted hardware for many configurations, exactly as in the prior art described in the introductory portion of the present application.

It is true that the PEs of Mirsky may themselves be combined, but not *to form* various functional units such as

an adder, ALU, multiplier, as claimed. Instead, the PEs of Mirsky with their included ALU, multiplier, and memory (see the abstract and Fig. 4 of Mirsky), may be combined to configure arbitrarily sized data paths and thereby extend the desired bit number of data processing (col. 7, line 59-col. 9, line 30). Because the resulting data paths may or may not utilize all of the individual functional units in a given PE, the apparatus disclosed by Mirsky has exactly the **same problem** as the apparatus described in the background section of the present application, which is that much of the hardware included in individual PEs may be wasted since the PEs themselves cannot be reconfigured. On the other hand, when the claimed invention is configured to act as a data path, and in particular a Very Long Instruction Word (VLIW) data path as recited in claim 19, the PEs of the claimed invention may be reconfigured into the specific functional units required of the data path, without any waste of hardware.

In summary, the claimed invention differs from the arrangement taught by Mirsky in the that the claimed invention includes:

- PEs that may be configured to form an adder, multiplier, or ALU,

Whereas the Mirsky patent teaches:

- PEs made up of an adder, multiplier, and ALU.

Because the Mirsky patent merely teaches the prior art discussed in the introductory portion of the present application, in which PEs made up of adders, multipliers, and ALUs are be combined to form data paths even though the individual adders, multipliers, or ALUs in the PEs may not all be needed, the Mirsky patent clearly does <u>not</u> anticipate the claimed invention and withdrawal of the

rejection of claims 1, 3,3, 7-16, and 18-20 under 35 USC §102(b) is respectfully requested.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the application are now believed to be in order, and such action is hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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